

What is claimed is:

- 1 1. A branch target prefetch apparatus comprising:
2 a presbyopic target buffer configured to receive a presbyopic target buffer
3 record, wherein the presbyopic target buffer record maps an entry location of a first
4 code region to an entry location of a second code region; and
5 a prefetch stream buffer configured to receive instructions from the second
6 code region responsive to an instruction pointer encountering the entry location of
7 the first code region.
- 1 2. The branch target prefetch apparatus of claim 1 wherein the presbyopic target
2 buffer is configured to receive the presbyopic target buffer record responsive to a
3 branch instruction being encountered in the first code region, the branch instruction
4 having a branch target address equal to the entry location of the second code region.
- 1 3. The branch target prefetch apparatus of claim 2 further comprising a branch
2 target buffer configured to receive a branch target buffer record that maps an address
3 of the branch instruction to the entry location of the second code region.
- 1 4. The branch target prefetch apparatus of claim 3 wherein the presbyopic target
2 buffer is configured to receive a plurality of presbyopic target buffer records, and is
3 further configured to be searched recursively.
- 1 5. The branch target prefetch apparatus of claim 4 wherein the prefetch stream
2 buffer is configured to receive instructions from a plurality of code regions
3 responsive to a recursive search of the presbyopic target buffer.
- 1 6. The branch target prefetch apparatus of claim 5 wherein the prefetch stream
2 buffer is configured to differentiate between instructions such that instructions from
3 different ones of the plurality of code regions can be invalidated.

1 7. The branch target prefetch apparatus of claim 3 wherein the branch target
2 buffer record includes a first confidence counter having a first number of bits, and
3 the presbyopic target buffer record includes a second confidence counter having a
4 second number of bits that is greater than the first number of bits.

1 8. The branch target prefetch apparatus of claim 1 wherein the presbyopic target
2 buffer record is configured to map the entry location of the first code region to entry
3 locations of a plurality of second code regions.

1 9. The branch target prefetch apparatus of claim 1 wherein a cache memory has
2 a cache latency associated therewith, and the prefetch target buffer has a depth at
3 least as deep as one cache latency.

1 10. A processor comprising:
2 a branch target buffer responsive to fetched instruction addresses, wherein the
3 branch target buffer is configured to map branch instruction addresses to branch
4 target addresses; and
5 a presbyopic target buffer responsive to the branch target buffer, wherein the
6 presbyopic target buffer is configured to map branch target addresses to subsequent
7 branch target addresses.

1 11. The processor of claim 10 further comprising:
2 a stream buffer configured to receive instructions fetched from subsequent
3 branch target addresses specified in the presbyopic target buffer.

1 12. The processor of claim 10 wherein the presbyopic target buffer is configured
2 to be recursively searched to predict a plurality of subsequent branch target
3 addresses.

1 13. The processor of claim 10 wherein the presbyopic target buffer implements
2 skip-adjacent mapping.

1 14. The processor of claim 10 wherein a complete branch target address is
2 specified by a fixed number of bits, and the presbyopic target buffer includes
3 mapping records that specify branch target addresses using less than the fixed
4 number of bits.

1 15. A processor comprising:
2 a branch target buffer responsive to fetched instruction addresses, wherein the
3 branch target buffer is configured to be searched for the fetched instruction addresses
4 and corresponding branch target addresses;
5 a presbyopic target buffer responsive to the branch target buffer, wherein the
6 presbyopic target buffer is configured to be searched for subsequent dynamic blocks
7 as a function of branch target addresses.

1 16. The processor of claim 15 wherein the presbyopic target buffer is configured
2 to map branch target addresses to subsequent dynamic block exit addresses.

1 17. The processor of claim 16 wherein the branch target buffer is further
2 responsive to subsequent dynamic block exit addresses from the presbyopic target
3 buffer.

1 18. The processor of claim 17 wherein the branch target buffer and presbyopic
2 target buffer are configured to be searched recursively in combination.

1 19. A processor comprising:
2 a first fetch buffer configured to receive instructions prefetched from
3 predicted branch target addresses; and

4 a second fetch buffer configured to receive instructions prefetched from
5 predicted subsequent blocks.

1 20. The processor of claim 19 wherein the second fetch buffer includes a coloring
2 field for each instruction included therein, such that each instruction included therein
3 can be assigned a color.

1 21. The processor of claim 19 wherein the second fetch buffer includes a
2 subsequent block demarcation mechanism to distinguish prefetched instructions from
3 different predicted subsequent blocks.

1 22. The processor of claim 19 further including a branch target buffer having
2 records that when populated, map branches to predicted branch targets.

1 23. The processor of claim 22 further including a presbyopic target buffer having
2 records that when populated, map predicted branch target addresses to predicted
3 subsequent blocks.

1 24. The processor of claim 23 wherein the presbyopic target buffer maps each
2 predicted branch target address to a plurality of predicted subsequent blocks.

1 25. The processor of claim 23 wherein the presbyopic target buffer is configured
2 to be recursively searched.

1 26. An instruction prefetch method comprising:
2 in a first buffer that maps branch instruction addresses to block entry
3 addresses, searching for a first buffer record having a branch instruction address that
4 matches a current instruction address;

5 when the first buffer record is found, searching a second buffer that maps
6 block entry addresses to subsequent block entry addresses for a second buffer record
7 having a block entry address matching the first buffer record; and
8 when the second buffer record is found, prefetching instructions beginning at
9 a subsequent block entry address included in the second buffer record.

1 27. The method of claim 26 wherein prefetching comprises entering instructions
2 into a stream buffer, the stream buffer having a coloring field for each instruction
3 entered.

1 28. The method of claim 26 further comprising:
2 searching the second buffer recursively; and
3 for each matching record found in the second buffer, each matching record
4 having a corresponding subsequent block entry address, prefetching instructions
5 from each of the corresponding subsequent block entry addresses.

1 29. The method of claim 28 wherein prefetching comprises:
2 entering instructions into a stream buffer, the stream buffer having a coloring
3 field for each instruction entered; and
4 assigning a different color to instructions fetched from different subsequent
5 block entry addresses.

1 30. The method of claim 29 wherein each recursive search represents a predicted
2 branch, the method further comprising flushing from the stream buffer instructions
3 prefetched as a result of a mispredicted branch.